IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:

Claus Dworski et al.

Examiner: Unknown

Serial No.:

10/564,650

Group Art Unit: Unknown

National Stage Filing Date: January 13, 2006

Docket: I431.144.101/FIN 503 PCT/US

Title:

ELECTRICAL CIRCUIT AND METHOD FOR TESTING ELECTRONIC

COMPONENT

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Dear Sir:

In compliance with the duty of disclosure under 37 C.F.R. § 1.56, it is respectfully requested that this Supplemental Information Disclosure Statement be entered and the documents listed on attached form 1449 be considered by the Examiner and made of record. Any required copies of patents, publications or other documents are enclosed for the Examiner's review. Pursuant to the provisions of M.P.E.P. 609, Applicant further requests a copy of the 1449 form, marked as being considered and initialled by the Examiner, be returned with the next Official Communication.

Since this Supplemental Information Disclosure Statement is being submitted within three months of filing national application; or date of entry of national application; or before the mailing date of the first Office Action on the merits, a fee has not been enclosed. However, if such fee is required, the Patent Office is hereby authorized to charge Deposit Account No. 500471 for fees as set forth under 37 C.F.R. 1.17(p).

Supplemental Information Disclosure Statement

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Applicant respectfully requests consideration of these references during prosecution of the above-identified matter. The Examiner is invited to contact the Applicant's representative at the below-listed telephone number if there are any questions regarding this Communication or the tendered references.

Respectfully submitted,

Claus Dworski et al.,

Ву,

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Dated: February 22, 2006

Steven E. Dicke Reg. No. 38,431

CERTIFICATE UNDER 37 C.F.R. 1.8: The undersigned hereby certifies that this paper or papers, as described herein, are being deposited in the United States Postal Service, as first class mail, in an envelope address to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 22 day of February, 2006.

Name: Steven E. Dicke



Docket No.: I431.144.101/FIN 503

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PCT/US

LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT

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U.S. PATENT DOCUMENTS Filing Date Document No. Sub Examiner If Appropriate Class Initial Name Class Date 08/2002 Mori et al. AA 2002/0105353 3,852,123 12/1974 Goltz AB 4,746,902 05/1988 Tol et al. AC 6,127,869 AD 10/2000 Hirasaka AE AF AG AH AI AJ AK AL FOREIGN PATENT DOCUMENTS Country **Translated** Document No. Class Sub Date Class Yes No 0 550 187 07/1993 **EPO** Yes AM Yes AN Yes AO OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.) A.K. Lu, G.W. Roberts, "An Analog Multi-Tone Signal Generator for Built-In Self-Test Applications", ITC 1994 AP Proceedings, Baltimore, USA Paper 27.3, pp. 650-659. A.K. Lu, G.W. Roberts, D.A. Johns, "A High-Quality Analog Oscillator Using Oversampling D/A Conversion AQ Techniques", ISCAS 1993 Proceedings, Chicago, May 1993, pp. 1298-1301. A.K. Lu, G.W. Roberts, D.A. Johns, "A High-Quality Analog Oscillator Using Oversampling D/A Conversion AR Techniques", IEEE Trans. On Circuits and Systems - II: Analog and Digital Signal Processing, Vol. 41, No. 7, July 1994. M. Hafed, G. Roberts, "Test and Evaluation of Multiple Embedded Mixed-Signal Test Cores", ITC 2002 Proceedings, AS Baltimore, USA, Paper 35.3, pp. 1022-1030. T.A. Rebold, F.H. Irons: "A phase-plane approach to the compensation of high-speed analog-to-digital converters" AT IEEE International Symposium on Circuits and Systems XP 008036387 Hofner T.C.: "INL/DNL Measurements for High-Speed ADCS" XP000947286 AU DATE CONSIDERED: **EXAMINER:**

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.